IN THE SPECIFICATION:

Please amend paragraph **[0014]** as follows:

[0014] FIGs. ~~1A-D~~ <u>1A–1D</u> illustrate a cross-sectional view of steps used in forming solder-receiving holes and channels in a substrate mold according to the present invention;

Please amend paragraph **[0021]** as follows:

[0021] FIG. 8 depicts a surface of a second embodiment of the substrate mold of the present invention having a plurality of hemispherical ~~cross-sectional shaped~~ <u>cross-sectional-shaped</u> cavities formed therein prior to the removal of the resist coating on the surface of the substrate mold;

Please amend paragraph **[0025]** as follows:

[0025] FIG. 12 depicts a surface of a third embodiment of the substrate mold of the present invention having a plurality of rectangular ~~cross-sectional shaped~~ <u>cross-sectional-shaped</u> cavities formed therein;

Please amend paragraph **[0032]** as follows:

[0032] Illustrated in drawing FIGS. 1A-1D is a method for fabricating the semiconductor substrate to form metal bumps or metal traces, or both, on the surface of a secondary substrate. A semiconductor substrate, typically a flat planar substrate having a flat planar upper surface, a flat planar lower surface, and a plurality of planar sides forming the periphery of the substrate, is selected to serve as a ~~bump-forming~~ <u>bump-and-trace-forming</u> substrate mold 10. The semiconductor substrate may be of any desired size and geometric shape suitable for use with an associated semiconductor device. The semiconductor substrate is selected from a semiconductor base material such as silicon, gallium arsenide, silicon on insulator, which may include silicon on glass or sapphire, or other well-known semiconductor substrate materials, as well as other similar types of materials, which are capable of being precisely micromachined and having a coefficient of thermal expansion (CTE) similar to that of

the semiconductor materials. In this particular application, it is preferred that a silicon substrate is used for substrate mold 10, although any of the other base materials may be freely substituted therefor. The silicon substrate is aligned such that the flat, planar upper surface 12 of substrate mold 10 defines the <100> plane of the substrate ~~mold 10~~ mold 10, which mates with a semiconductor device (not shown). As is shown in drawing Fig. 1A, the flat, planar upper surface 12 of substrate ~~mold 10~~ mold 10, the <100> plane, has a first protective mask layer 14 located thereon. The first protective mask layer 14 serves to protect the surface of substrate mold 10 when a subsequent etch is performed to make the cavities or apertures in the flat, planar upper surface 12. First protective mask layer 14 may be selected from particular etch-resistant materials such as nitride, oxide, or a hardened polymer spin-on mask. Substrate mold 10 typically has a thickness of about 25 to 28 mils.

Please amend paragraph **[0035]** as follows:

[0035] Although drawing FIGS. ~~1A-D~~ 1A–1D illustrate only a single cavity 18, it is intended that a plurality of cavities be formed in an array across substrate mold 10. An example of a solder ball-forming mold or trace-forming substrate mold 10 that has such a plurality of cavities 18 is depicted in drawing FIG. 2. Release layer 20 (FIG. 1D) is applied and utilized to minimize the wetting of solder paste on the substrate mold 10 when the assembly is heated in order to transfer the solder onto the bumps of the secondary surface.

Please amend paragraph **[0038]** as follows:

[0038] Once the metal solder paste 24 is applied to flat, planar upper surface 12 of substrate mold 10, the entire assembly is heated to a temperature sufficient enough to slightly melt the metal solder paste 24 in order to begin the formation of the solder bumps 26 to be transferred. As shown in drawing FIG. 4, after this partially melted solder state has been reached, substrate mold 10 is inverted and applied to the surface of a carrier substrate 28, which may comprise a semiconductor device (die), wafer, or flexible substrate, such as a flex tape. The assembly of the substrate mold 10 and carrier substrate 28 is heated to a sufficiently high enough

temperature to cause solder bumps 26 to slightly reflow and release from the release layer 20 formed on substrate mold 10. Substrate mold 10 is then removed and solder bumps 26 adhere to bond pads, terminal pads or other ~~solder wettable~~ solder-wettable conductive sites 30 on carrier substrate 28, as shown in drawing FIG. 5. Next, an additional reflow step may be performed that causes solder bumps 26 to form into approximately spherically shaped solder balls 32 attached to ~~solder wettable~~ solder-wettable conductive sites 30 as depicted in drawing FIG. 6.

Please amend paragraph **[0040]** as follows:

[0040] Although it has been depicted how spherically shaped solder balls 32 or bumps are formed in drawing FIG. 4, it is also possible to form cavities 18 and metal traces using substrate mold 10. The same type of patterning and etch steps as described with respect to FIGS. 1A-1B would be followed, but would include a layout that would form metal traces or channels.

Please amend paragraph **[0042]** as follows:

[0042] Referring to drawing Fig. 8, an alternative embodiment of a substrate mold 40 of the present invention is illustrated. The substrate mold 40 is similar to the substrate mold 10 described hereinbefore as to construction and methods of ~~construction~~ construction, except that the cavities 18 formed therein are hemispherically shaped. As illustrated, the first protective mask layer 14 used to form the plurality of cavities 18 is present on portions of the flat, planar upper surface 42 of the substrate mold 40. As with the substrate mold 10, the substrate mold 40 may include a release layer 20 to aid in the release of the solder paste contained within the hemispherical cavities 18.

Please amend paragraph **[0043]** as follows:

[0043] Referring to drawing Fig. 9, once the metal solder paste 24 is applied to flat, planar upper surface 42 of substrate mold 40, as described herein with respect to substrate mold 10 illustrated in drawing Fig. 3, the entire assembly of the substrate mold 40 and carrier

substrate 28 having ~~solder wettable~~ solder-wettable conductive sites 30 or bond pads located thereon for the metal solder paste 24 to be applied is heated to a temperature sufficient enough to slightly melt the metal solder paste 24 in order to begin the formation of the solder bumps 26 to be transferred.

Please amend paragraph **[0044]** as follows:

[0044] As shown in drawing FIG. 9, after this partially melted solder state has been reached, the assembly of the substrate mold 40 and the carrier substrate 28 is inverted so that the metal solder paste 24 in cavities 18 is applied to the ~~solder wettable~~ solder-wettable conductive sites 30 on the surface of the carrier substrate 28, which may comprise a semiconductor device (die), wafer, or flexible substrate, such as a flex tape. The assembly of the substrate mold 40 and carrier substrate 28 is heated to a sufficiently high enough temperature to cause solder bumps 26 to slightly reflow and release from the release layer 20 formed on substrate mold 40. Substrate mold 40 is then removed and solder bumps 26 adhere to the conductive sites, bond pads, terminal pads or other ~~solder wettable~~ solder-wettable conductive sites 30 on carrier substrate 28, as shown in drawing FIG. 10. Next, an additional reflow step may be performed that causes solder bumps 26 to form into approximately spherically shaped solder balls 32 attached to ~~solder wettable~~ solder-wettable conductive sites 30 as depicted in drawing FIG. 11.

Please amend paragraph **[0046]** as follows:

[0046] Referring to drawing Fig. 12, an alternative embodiment of a substrate mold 50 of the present invention is illustrated. The substrate mold 50 is similar to the substrate molds 10 and 40 described hereinbefore as to construction and methods of construction except that the cavities 18 formed therein are generally rectangular, or square shaped (shown in dashed lines). The first protective mask layer 14 used to form the plurality of cavities 18 present on portions of the flat, planar upper surface 42 of the substrate mold 50 is not illustrated. As with the substrate mold 10, the substrate mold 50 may include a release layer 20 (FIG. 13) to aid in the release of the solder paste contained within the ~~hemispherical~~ rectangular or square-shaped cavities 18.

Referring to drawing Fig. 13, once the metal solder paste 24 is applied to flat, planar upper surface 42 of substrate mold 50, as described herein with respect to substrate mold 10 illustrated in drawing Fig. 3, the entire assembly of the substrate mold 50 and carrier substrate 28 having ~~solder wettable~~ solder-wettable conductive sites 30 or bond pads located thereon for the metal solder paste 24 to be applied is heated to a temperature sufficiently high enough to slightly melt the metal solder paste 24 in order to begin the formation of the solder bumps 26 to be transferred.

Please amend paragraph **[0047]** as follows:

[0047] As shown in drawing FIG. 13, after this partially melted solder state has been reached, the assembly of the substrate mold 50 and the carrier substrate 28 is inverted so that the metal solder paste 24 is applied to the ~~solder wettable~~ solder-wettable conductive sites 30 on the surface of the carrier substrate 28, which may comprise a semiconductor device (die), wafer, or flexible substrate, such as a flex tape. The assembly of the substrate mold 50 and carrier substrate 28 is heated to a sufficiently high enough temperature to cause solder bumps 26 to slightly reflow and release from the release layer 20 formed on substrate mold 50. Substrate mold 50 is then removed and solder bumps 26 adhere to the conductive sites, bond pads, terminal pads or other ~~solder wettable~~ solder-wettable conductive sites 30 on carrier substrate 28, as shown in drawing FIG. 14. Next, an additional reflow step may be performed that causes solder bumps 26 to form into approximately spherically shaped solder balls 32 attached to ~~solder wettable~~ solder-wettable conductive sites 30 as depicted in drawing FIG. 15.

Please amend paragraph **[0050]** as follows:

[0050] Referring to drawing Fig. 17, the substrate mold 100 is illustrated having metal solder paste 24 located in cavities 18 having release layer 20 therein. After the metal solder paste 24 is placed in the cavities 18, a carrier substrate 28 (see Fig. 4) is applied to the substrate mold 100, the assembly of the substrate mold 100 and carrier substrate 28 inverted, and the electrical resistance heating strips 66 on the substrate mold 100 actuated to heat the metal solder paste 24 to transfer the same to the carrier substrate 28. After the metal solder paste 24 is

transferred to the carrier substrate 28, the carrier substrate 28 is further heated to cause the solder paste to adhere to the~~ solder wettable~~ solder-wettable conductive sites 30 on the carrier substrate 28 to substantially form spherically shaped solder balls 32 thereon.

Please amend paragraph **[0052]** as follows:

[0052] Substrate molds 10, 40, 50 and 100 described herein are useful in forming contact bumps for many applications. One application is the formation of flexible connecting tape that requires bumps for interconnection of traces on the tape to a die or other element. The micromachining of substrate mold 10 provides a much more accurate means for placing the solder ball-shaped bumps over the prior art methods of merely placing bumps on top of a screen and then having the screen place the bumps in a proper alignment. Further, the solder ball-shaped bumps have a more uniform volume and shape as the cavity dimensions in the semiconductor mold provide a substantially precise control over the formation of the solder ball-shaped bumps. By contrast, in the prior art, the uniformity of solder balls has always been a problem, especially at the smaller diameter dimensions that are now being used. Another application for the present invention is for the direct placement of the solder ball-shaped bumps on a semiconductor device or die for attachment. Yet another application includes placing the solder ball-shaped bumps on a wafer-scale device for interconnection. This allows multiple devices placed on the same substrate to be interconnected using the precision of the solder ball-shaped bumps. For example, the solder ball-shaped bump application is useful in chip scale packages (CSP) or in fine ball grid array (FBGA) packages. The~~ in situ~~ *in situ* electrical resistance heating strip allows for selecting which balls need to be transferred by selectively heating only those electrical resistance heating strips 66.